

MEMORY

CMOS

1 M × 16 BIT

FAST PAGE MODE DYNAMIC RAM

MB8118160B-50/-60

CMOS 1,048,576 × 16 Bit Fast Page Mode Dynamic RAM

■ DESCRIPTION

The Fujitsu MB8118160B is a fully decoded CMOS Dynamic RAM (DRAM) that contains 16,777,216 memory cells accessible in 16-bit increments. The MB8118160B features a "fast page" mode of operation whereby high-speed random access of up to 1,024 × 16 bits of data within the same row can be selected. The MB8118160B DRAM is ideally suited for mainframe, buffers, hand-held computers video imaging equipment, and other memory applications where very low power dissipation and high bandwidth are basic requirements of the design. Since the standby current of the MB8118160B is very small, the device can be used as a non-volatile memory in equipment that uses batteries for primary and/or auxiliary power.

The MB8118160B is fabricated using silicon gate CMOS and Fujitsu's advanced four-layer polysilicon and two-layer aluminum process. This process, coupled with advanced stacked capacitor memory cells, reduces the possibility of soft errors and extends the time interval between memory refreshes. Clock timing requirements for the MB8118160B are not critical and all inputs are TTL compatible.

■ PRODUCT LINE & FEATURES

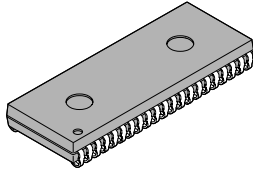
Parameter		MB8118160B-50	MB8118160B-60
RAS Access Time		50 ns max.	60 ns max.
Random Cycle Time		90 ns min.	110 ns min.
Address Access Time		25 ns max.	30 ns max.
CAS Access Time		15 ns max.	15 ns max.
Fast Page Mode Cycle Time		35 ns min.	40 ns min.
Low Power Dissipation	Operating current	990 mW max.	825 mW max.
	Standby current	11 mW max. (TTL level)/5.5 mW max. (CMOS level)	

- 1,048,576 words × 16 bit organization
- Silicon gate, CMOS, Advanced Stacked Capacitor Cell
- All input and output are TTL compatible
- 1,024 refresh cycles every 16.4 ms
- Early write or \overline{OE} controlled write capability
- \overline{RAS} -only, \overline{CAS} -before- \overline{RAS} , or Hidden Refresh
- Fast page mode, Read-Modify-Write capability
- On chip substrate bias generator for high performance

MB8118160B-50/-60

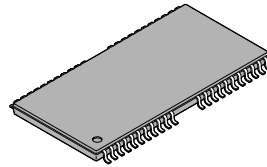
■ PACKAGE

Plastic SOJ Package



(LCC-42P-M01)

Plastic TSOP(II) Package



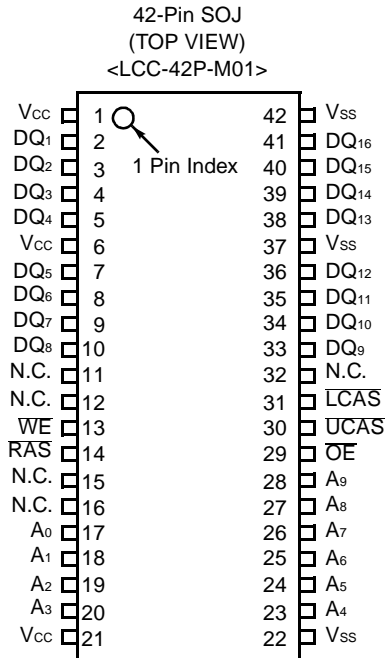
(FPT-50P-M06)
(Normal Bend)

Package and Ordering Information

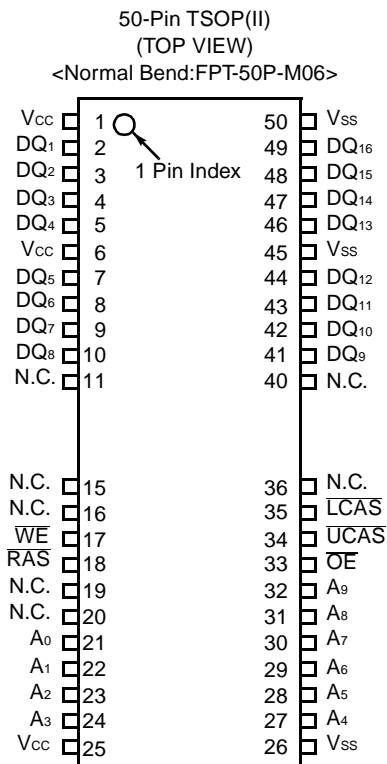
- 42-pin plastic (400 mil) SOJ, order as MB8118160B-xxPJ
- 50-pin plastic (400 mil) TSOP(II) with normal bend leads, order as MB8118160B-xxPFTN

MB8118160B-50/-60

■ PIN ASSIGNMENTS AND DESCRIPTIONS

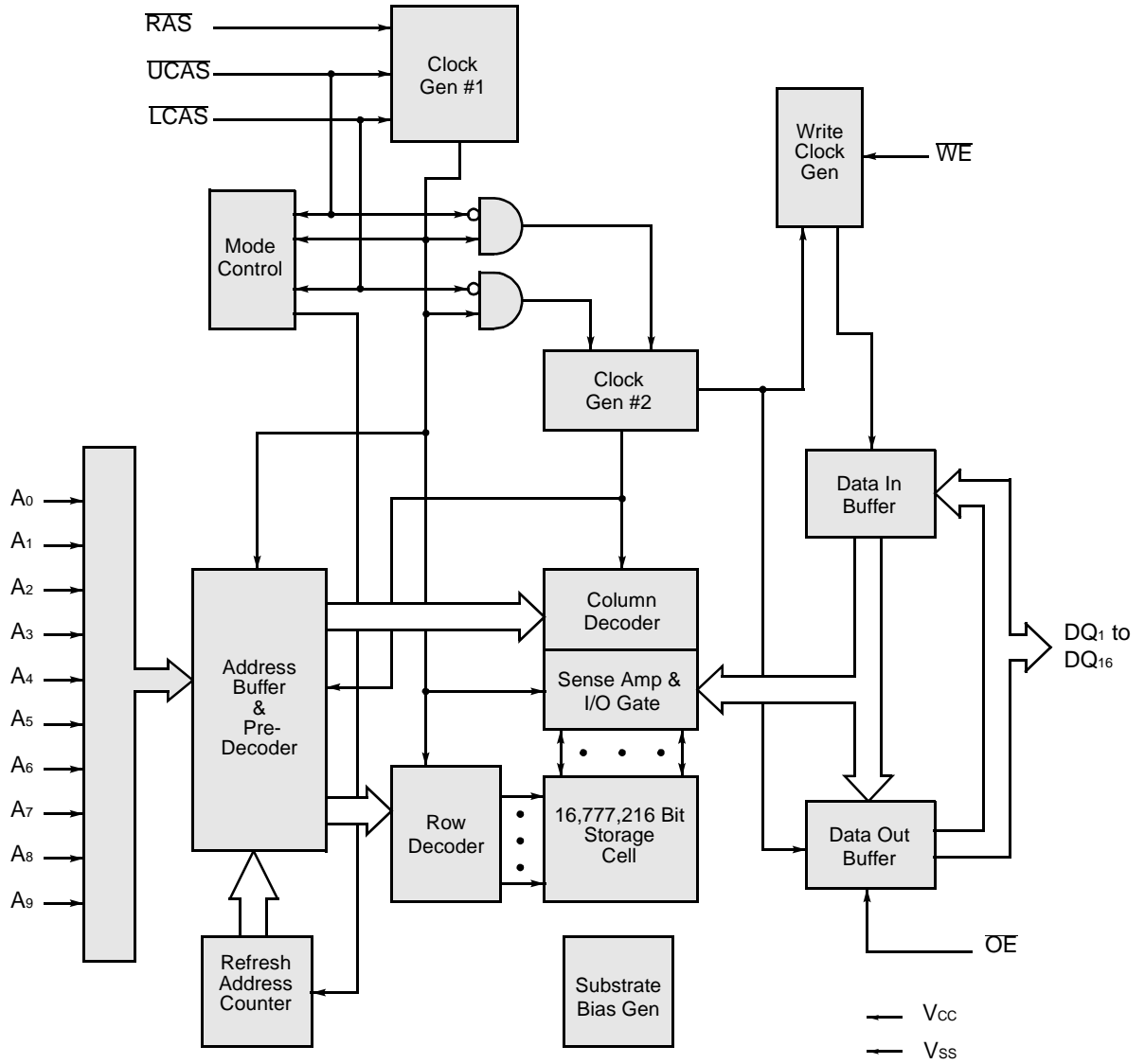


Designator	Function
A ₀ to A ₉	Address inputs row : A ₀ to A ₉ column : A ₀ to A ₉ refresh : A ₀ to A ₉
RAS	Row address strobe
LCAS	Lower column address strobe
UCAS	Upper column address strobe
WE	Write enable
OE	Output enable
DQ ₁ to DQ ₁₆	Data Input/Output
V _{CC}	+5.0 volt power supply
V _{SS}	Circuit ground
N.C.	No connection



MB8118160B-50/-60

Fig. 1 - MB8118160B DYNAMIC RAM - BLOCK DIAGRAM



FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input					Address Input		Input/Output Data				Refresh	Note
	RAS	LCAS	UCAS	WE	OE	Row	Column	DQ ₁ to DQ ₈		DQ ₉ to DQ ₁₆			
								Input	Output	Input	Output		
Standby	H	H	H	X	X	—	—	—	High-Z	—	High-Z	—	
Read Cycle	L	L H L	H L L	H	L	Valid	Valid	—	Valid High-Z Valid	—	High-Z Valid Valid	Yes*	$t_{RCS} \geq t_{RCS}$ (min.)
Write Cycle (Early Write)	L	L H L	H L L	L	X	Valid	Valid	Valid — Valid	High-Z	— Valid Valid	High-Z	Yes*	$t_{WCS} \geq t_{WCS}$ (min.)
Read-Modify- Write Cycle	L	L H L	H L L	H→L	L→H	Valid	Valid	Valid — Valid	Valid High-Z Valid	— Valid Valid	High-Z Valid Valid	Yes*	
RAS-only Refresh Cycle	L	H	H	X	X	Valid	X	—	High-Z	—	High-Z	Yes	
CAS-before- RAS Refresh Cycle	L	L	L	X	X	X	X	—	High-Z	—	High-Z	Yes	$t_{CSR} \geq t_{CSR}$ (min.)
Hidden Refresh Cycle	H→L	L H L	H L L	H→X	L	X	X	—	Valid High-Z Valid	—	High-Z Valid Valid	Yes	Previous data is kept

X: "H" or "L"

*: It is impossible in Fast Page Mode.

FUNCTIONAL OPERATION

ADDRESS INPUTS

Twenty input bits are required to decode any sixteen of 16,777,216 cell addresses in the memory matrix. Since only twelve address bits (A₀ to A₉) are available, the column and row inputs are separately strobed by LCAS or UCAS and RAS as shown in Figure 1. First, ten row address bits are input on pins A₀-through-A₉ and latched with the row address strobe (RAS) then, ten column address bits are input and latched with the column address strobe (LCAS or UCAS). Both row and column addresses must be stable on or before the falling edges of RAS and LCAS or UCAS, respectively. The address latches are of the flow-through type; thus, address information appearing after t_{RAH} (min.) + t_T is automatically treated as the column address.

WRITE ENABLE

The read or write mode is determined by the logic state of WE. When WE is active Low, a write cycle is initiated; when WE is High, a read cycle is selected. During the read mode, input data is ignored.

DATA INPUTS

Input data is written into memory in either of three basic ways – an early write cycle, an OE (delayed) write cycle, and a read-modify-write cycle. The falling edge of WE or LCAS / UCAS, whichever is later, serves as the input data-latch strobe. In an early write cycle, the input data of DQ₁ to DQ₈ is strobed by LCAS and DQ₉ to DQ₁₆ is strobed by UCAS and the setup/hold times are referenced to each LCAS and UCAS because WE goes Low before LCAS / UCAS. In a delayed write or a read-modify-write cycle, WE goes Low after LCAS / UCAS; thus, input data is strobed by WE and all setup/hold times are referenced to the write-enable signal.

MB8118160B-50/-60

DATA OUTPUTS

The three-state buffers are TTL compatible with a fanout of two TTL loads. Polarity of the output data is identical to that of the input; the output buffers remain in the high-impedance state until the column address strobe goes Low. When a read or read-modify-write cycle is executed, valid outputs are obtained under the following conditions:

- t_{RAC}** : from the falling edge of \overline{RAS} when t_{RCD} (max.) is satisfied.
- t_{CAC}** : from the falling edge of \overline{LCAS} (for DQ₁ to DQ₈) \overline{UCAS} (for DQ₉ to DQ₁₆) when t_{RCD} is greater than t_{RCD} (max.).
- t_{AA}** : from column address input when t_{RAD} is greater than t_{RAD} (max.).
- t_{OEA}** : from the falling edge of \overline{OE} when \overline{OE} is brought Low after t_{RAC}, t_{CAC}, or t_{AA}, and t_{RCD} (max.) is satisfied.

The data remains valid until either \overline{LCAS} / \overline{UCAS} or \overline{OE} returns to a High logic level. When an early write is executed, the output buffers remain in a high-impedance state during the entire cycle.

FAST PAGE MODE OF OPERATION

The fast page mode of operation provides faster memory access and lower power dissipation. The fast page mode is implemented by keeping the same row address and strobing in successive column addresses. To satisfy these conditions, \overline{RAS} is held Low for all contiguous memory cycles in which row addresses are common. For each fast page of memory, any of 1,024 × 16 bits can be accessed and, when multiple MB8118160Bs are used, \overline{CAS} is decoded to select the desired memory fast page. Fast page mode operations need not be addressed sequentially and combinations of read, write, and/or read-modify-write cycles are permitted.

MB8118160B-50/-60

■ ABSOLUTE MAXIMUM RATINGS (See WARNING)

Parameter	Symbol	Value	Unit
Voltage at Any Pin Relative to V _{SS}	V _{IN} , V _{OUT}	-0.5 to +7.0	V
Voltage of V _{CC} Supply Relative to V _{SS}	V _{CC}	-0.5 to +7.0	V
Power Dissipation	P _D	1.0	W
Short Circuit Output Current	I _{OUT}	-50 to +50	mA
Operating Temperature	T _{OP}	0 to +70	°C
Storage Temperature	T _{STG}	-55 to +125	°C

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Notes	Symbol	Min.	Typ.	Max.	Unit	Ambient Operating Temp.
Supply Voltage	*1	V _{CC}	4.5	5.0	5.5	V	0°C to +70°C
		V _{SS}	0.0	0.0	0.0		
Input High Voltage, All Inputs	*1	V _{IH}	2.4	—	6.5	V	
Input Low Voltage, All Inputs*	*1	V _{IL}	-0.3	—	0.8	V	

* : Undershoots of up to -2.0 volts with a pulse width not exceeding 20 ns are acceptable.

WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

■ CAPACITANCE

(T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Max.	Unit
Input Capacitance, A ₀ to A ₉	C _{IN1}	5	pF
Input Capacitance, $\overline{\text{RAS}}$, $\overline{\text{LCAS}}$, $\overline{\text{UCAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$	C _{IN2}	5	pF
Input/Output Capacitance, DQ ₁ to DQ ₁₆	C _{DQ}	7	pF

MB8118160B-50/-60

■ DC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.)

Note 3

Parameter	Notes	Symbol	Conditions	Value			Unit	
				Min.	Typ.	Max.		
Output High Voltage	*1	V_{OH}	$I_{OH} = -5.0 \text{ mA}$	2.4	—	—	V	
Output Low Voltage	*1	V_{OL}	$I_{OL} = +4.2 \text{ mA}$	—	—	0.4		
Input Leakage Current (Any Input)		$I_{I(L)}$	$0 \text{ V} \leq V_{IN} \leq V_{CC}$; $4.5 \text{ V} \leq V_{CC} \leq 5.5 \text{ V}$; $V_{SS} = 0 \text{ V}$; All other pins not under test = 0 V	-10	—	10	μA	
Output Leakage Current		$I_{DQ(L)}$	$0 \text{ V} \leq V_{OUT} \leq V_{CC}$; $4.5 \text{ V} \leq V_{CC} \leq 5.5 \text{ V}$; Data out disabled	-10	—	10		
Operating Current (Average Power Supply Current)	*2	MB8118160B-50	I_{CC1}	RAS & LCAS, UCAS cycling; $t_{RC} = \text{min}$	—	—	180	mA
		MB8118160B-60					150	
Standby Current (Power Supply Current)	*2	TTL level	I_{CC2}	RAS = LCAS = UCAS = V_{IH}	—	—	2.0	mA
		CMOS level					RAS = LCAS = UCAS \geq $V_{CC} - 0.2 \text{ V}$	
Refresh Current #1 (Average Power Supply Current)	*2	MB8118160B-50	I_{CC3}	LCAS = UCAS = V_{IH} , RAS cycling; $t_{RC} = \text{min}$	—	—	180	mA
		MB8118160B-60					150	
Fast Page Mode Current	*2	MB8118160B-50	I_{CC4}	RAS = V_{IL} , LCAS = UCAS cycling; $t_{HPC} = \text{min}$	—	—	110	mA
		MB8118160B-60					100	
Refresh Current #2 (Average Power Supply Current)	*2	MB8118160B-50	I_{CC5}	RAS cycling; CAS-before-RAS; $t_{RC} = \text{min}$	—	—	180	mA
		MB8118160B-60					150	

MB8118160B-50/-60

■ AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.)

Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB8118160B-50		MB8118160B-60		Unit
				Min.	Max.	Min.	Max.	
1	Time Between Refresh		t _{REF}	—	16.4	—	16.4	ms
2	Random Read/Write Cycle Time		t _{RC}	90	—	110	—	ns
3	Read-Modify-Write Cycle Time		t _{RWC}	126	—	150	—	ns
4	Access Time from $\overline{\text{RAS}}$	*6,9	t _{RAC}	—	50	—	60	ns
5	Access Time from $\overline{\text{CAS}}$	*7,9	t _{CAC}	—	15	—	15	ns
6	Column Address Access Time	*8,9	t _{AA}	—	25	—	30	ns
7	Output Hold Time		t _{OH}	3	—	3	—	ns
8	Output Buffer Turn On Delay Time		t _{ON}	0	—	0	—	ns
9	Output Buffer Turn Off Delay Time	*10	t _{OFF}	—	13	—	15	ns
10	Transition Time		t _r	3	50	3	50	ns
11	$\overline{\text{RAS}}$ Precharge Time		t _{RP}	30	—	40	—	ns
12	$\overline{\text{RAS}}$ Pulse Width		t _{RAS}	50	100000	60	100000	ns
13	$\overline{\text{RAS}}$ Hold Time		t _{RSH}	15	—	15	—	ns
14	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time		t _{CRP}	5	—	5	—	ns
15	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	*11,12	t _{RCD}	17	35	20	45	ns
16	$\overline{\text{CAS}}$ Pulse Width		t _{CAS}	15	—	15	—	ns
17	$\overline{\text{CAS}}$ Hold Time		t _{CSH}	50	—	60	—	ns
18	$\overline{\text{CAS}}$ Precharge Time (Normal)	*19	t _{CPN}	7	—	10	—	ns
19	Row Address Setup Time		t _{ASR}	0	—	0	—	ns
20	Row Address Hold Time		t _{RAH}	7	—	10	—	ns
21	Column Address Setup Time		t _{ASC}	0	—	0	—	ns
22	Column Address Hold Time		t _{CAH}	7	—	10	—	ns
23	Column Address Hold Time from $\overline{\text{RAS}}$		t _{AR}	24	—	30	—	ns
24	$\overline{\text{RAS}}$ to Column Address Delay Time	*13	t _{RAD}	12	25	15	30	ns
25	Column Address to $\overline{\text{RAS}}$ Lead Time		t _{RAL}	25	—	30	—	ns
26	Column Address to $\overline{\text{CAS}}$ Lead Time		t _{CAL}	25	—	30	—	ns
27	Read Command Setup Time		t _{RCS}	0	—	0	—	ns
28	Read Command Hold Time Referenced to $\overline{\text{RAS}}$	*14	t _{RRH}	0	—	0	—	ns
29	Read Command Hold Time Referenced to $\overline{\text{CAS}}$	*14	t _{RCH}	0	—	0	—	ns
30	Write Command Setup Time	*15,20	t _{WCS}	0	—	0	—	ns
31	Write Command Hold Time		t _{WCH}	7	—	10	—	ns
32	Write Command Hold Time from $\overline{\text{RAS}}$		t _{WCR}	24	—	30	—	ns

(Continued)

MB8118160B-50/-60

(Continued)

No.	Parameter	Notes	Symbol	MB8118160B-50		MB8118160B-60		Unit
				Min.	Max.	Min.	Max.	
33	\overline{WE} Pulse Width		tWP	7	—	10	—	ns
34	Write Command to \overline{RAS} Lead Time		tRWL	13	—	15	—	ns
35	Write Command to \overline{CAS} Lead Time		tCWL	15	—	15	—	ns
36	DIN Setup Time		tDS	0	—	0	—	ns
37	DIN Hold Time		tDH	7	—	10	—	ns
38	Data Hold Time from \overline{RAS}		tDHR	24	—	30	—	ns
39	\overline{RAS} to \overline{WE} Delay Time	*20	tRWD	68	—	80	—	ns
40	\overline{CAS} to \overline{WE} Delay Time	*20	tCWD	31	—	35	—	ns
41	Column Address to \overline{WE} Delay Time	*20	tAWD	43	—	50	—	ns
42	\overline{RAS} Precharge Time to \overline{CAS} Active Time (Refresh Cycles)		tRPC	5	—	5	—	ns
43	\overline{CAS} Setup Time for \overline{CAS} -before- \overline{RAS} Refresh		tCSR	0	—	0	—	ns
44	\overline{CAS} Hold Time for \overline{CAS} -before- \overline{RAS} Refresh		tCHR	10	—	10	—	ns
45	Access Time from \overline{OE}	*9	tOEA	—	15	—	15	ns
46	Output Buffer Turn Off Delay from \overline{OE}	*10	tOEZ	—	13	—	15	ns
47	\overline{OE} to \overline{RAS} Lead Time for Valid Data		tOEL	5	—	5	—	ns
48	\overline{OE} Hold Time Referenced to \overline{WE}	*16	tOEH	5	—	5	—	ns
49	\overline{OE} to Data in Delay Time		tOED	13	—	15	—	ns
50	\overline{CAS} to Data in Delay Time		tCDD	13	—	15	—	ns
51	DIN to \overline{CAS} Delay Time	*17	tDZC	0	—	0	—	ns
52	DIN to \overline{OE} Delay Time	*17	tDZO	0	—	0	—	ns
53	Fast Page Mode \overline{RAS} Pulse Width		tRASP	—	10000	—	10000	ns
54	Fast Page Mode Read/Write Cycle Time		tPC	35	—	40	—	ns
55	Fast Page Mode Read-Modify-Write Cycle Time		tPRWC	73	—	80	—	ns
56	Access Time from \overline{CAS} Precharge	*9,18	tCPA	—	30	—	35	ns
57	Fast Page Mode \overline{CAS} Precharge Time		tCP	7	—	10	—	ns
58	Fast Page Mode \overline{RAS} Hold Time from \overline{CAS} Precharge		tRHCP	30	—	35	—	ns
59	Fast Page Mode \overline{CAS} Precharge to \overline{WE} Delay Time	*20	tCPWD	48	—	55	—	ns

- Notes:**
- *1. Referenced to V_{SS} .
 - *2. I_{CC} depends on the output load conditions and cycle rates; the specified values are obtained with the output open.
 I_{CC} depends on the number of address change as $\overline{RAS} = V_{IL}$, $\overline{UCAS} = V_{IH}$, $\overline{LCAS} = V_{IH}$ and $V_{IL} > -0.3$ V. I_{CC1} , I_{CC3} , I_{CC4} and I_{CC5} are specified at one time of address change during $\overline{RAS} = V_{IL}$ and $\overline{UCAS} = V_{IH}$, $\overline{LCAS} = V_{IH}$. I_{CC2} is specified during $\overline{RAS} = V_{IH}$ and $V_{IL} > -0.3$ V.
 - *3. An initial pause ($\overline{RAS} = \overline{CAS} = V_{IH}$) of 200 μ s is required after power-up followed by any eight \overline{RAS} -only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight \overline{CAS} -before- \overline{RAS} initialization cycles instead of 8 \overline{RAS} cycles are required.
 - *4. AC characteristics assume $t_t = 5$ ns.
 - *5. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also transition times are measured between V_{IH} (min.) and V_{IL} (max.).
 - *6. Assumes that $t_{RCD} \leq t_{RCD}(\text{max.})$, $t_{RAD} \leq t_{RAD}(\text{max.})$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown. Refer to Fig. 2 and 3.
 - *7. If $t_{RCD} \geq t_{RCD}(\text{max.})$, $t_{RAD} \geq t_{RAD}(\text{max.})$, and $t_{ASC} \geq t_{AA} - t_{CAC} - t_t$, access time is t_{CAC} .
 - *8. If $t_{RAD} \geq t_{RAD}(\text{max.})$ and $t_{ASC} \leq t_{AA} - t_{CAC} - t_t$, access time is t_{AA} .
 - *9. Measured with a load equivalent to two TTL loads and 100 pF.
 - *10. t_{OFF} and t_{OEZ} are specified that output buffer change to high-impedance state.
 - *11. Operation within the $t_{RCD}(\text{max.})$ limit ensures that $t_{RAC}(\text{max.})$ can be met. $t_{RCD}(\text{max.})$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{RCD}(\text{max.})$ limit, access time is controlled exclusively by t_{CAC} or t_{AA} .
 - *12. $t_{RCD}(\text{min.}) = t_{RAH}(\text{min.}) + 2t_t + t_{ASC}(\text{min.})$.
 - *13. Operation within the $t_{RAD}(\text{max.})$ limit ensures that $t_{RAC}(\text{max.})$ can be met. $t_{RAD}(\text{max.})$ is specified as a reference point only; if t_{RAD} is greater than the specified $t_{RAD}(\text{max.})$ limit, access time is controlled exclusively by t_{CAC} or t_{AA} .
 - *14. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
 - *15. t_{WCS} is specified as a reference point only. If $t_{WCS} \geq t_{WCS}(\text{min.})$ the data output pin will remain High-Z state through entire cycle.
 - *16. Assumes that $t_{WCS} < t_{WCS}(\text{min.})$.
 - *17. Either t_{DZC} or t_{DZO} must be satisfied.
 - *18. t_{CPA} is access time from the selection of a new column address (that is caused by changing both \overline{UCAS} and \overline{LCAS} from "L" to "H"). Therefore, if t_{CP} is long, t_{CPA} is longer than $t_{CPA}(\text{max.})$.
 - *19. Assumes that \overline{CAS} -before- \overline{RAS} refresh.
 - *20. t_{WCS} , t_{CWD} , t_{RWD} , t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as an electrical characteristic only. If $t_{WCS} \geq t_{WCS}(\text{min.})$, the cycle is an early write cycle and DQ pin will maintain high-impedance state throughout the entire cycle. If $t_{CWD} \geq t_{CWD}(\text{min.})$, $t_{RWD} \geq t_{RWD}(\text{min.})$, and $t_{AWD} \geq t_{AWD}(\text{min.})$, $t_{CPWD} \geq t_{CPWD}(\text{min.})$, the cycle is a read-modify-write cycle and data from the selected cell will appear at the DQ pin. If neither of the above conditions is satisfied, the cycle is a delayed write cycle and invalid data will appear the DQ pin, and write operation can be executed by satisfying t_{RWL} , t_{CWL} , t_{RAL} , and t_{CAL} specifications.

MB8118160B-50/-60

Fig. 2 – t_{RAC} vs. t_{RCD}

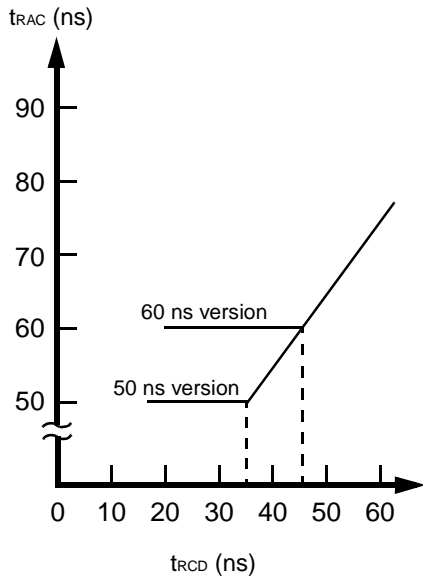


Fig. 3 – t_{RAC} vs. t_{RAD}

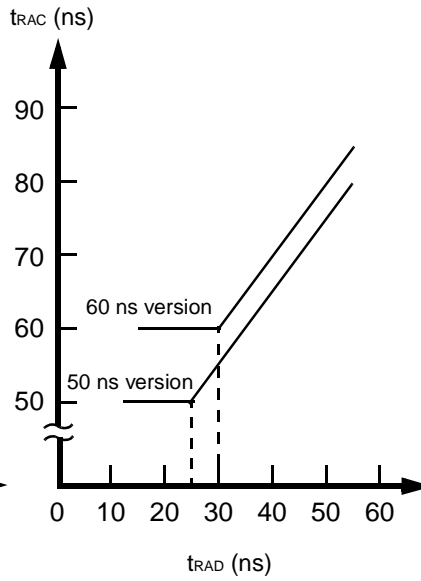


Fig. 4 – t_{CPA} vs. t_{CP}

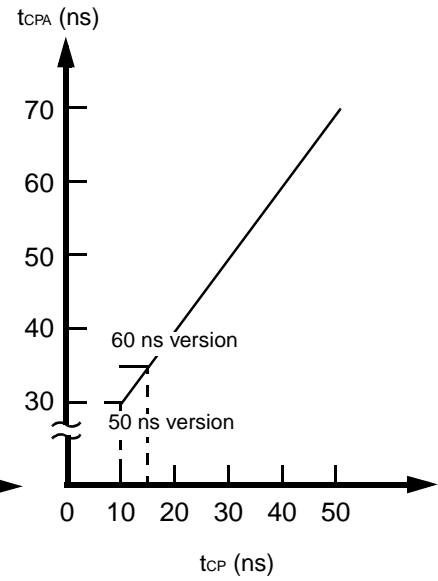
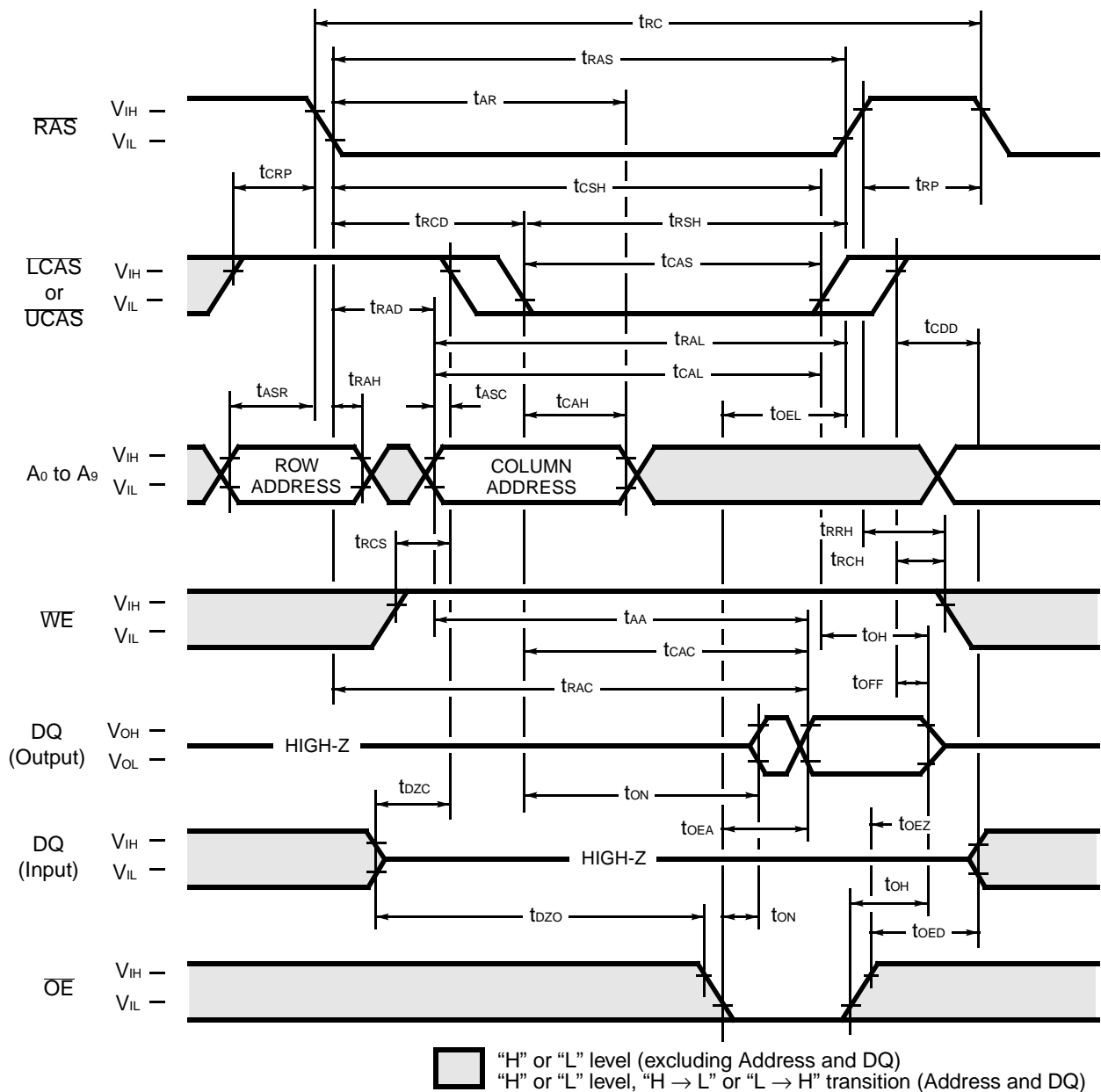


Fig. 5 – READ CYCLE

**DESCRIPTION**

To implement a read operation, a valid address is latched by the RAS and LCAS or UCAS address strobes and with WE set to a High level and OE set to a low level, the output is valid once the memory access time has elapsed. LCAS controls the input/output data on DQ₁ to DQ₈ pins, UCAS controls the input/output data on DQ₈ to DQ₁₆ pins. The access time is determined by RAS(t_{RAC}), LCAS/UCAS(t_{CAC}), OE(t_{OE}) or column addresses (t_{AA}) under the following conditions:

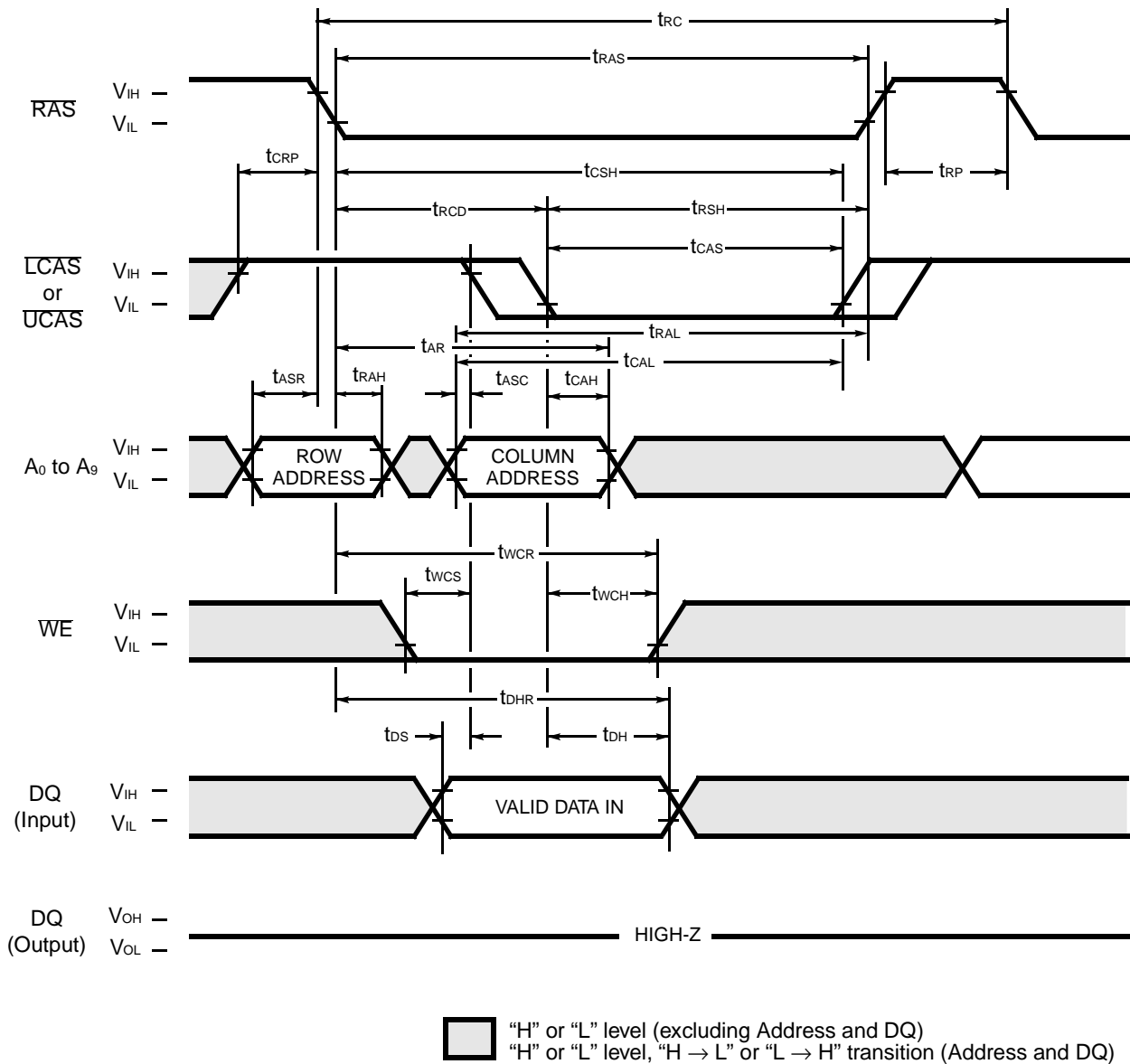
If t_{RCD} > t_{RCD(max.)}, access time = t_{CAC}.

If t_{TRAD} > t_{TRAD(max.)}, access time = t_{AA}.

If OE is brought Low after t_{RAC}, t_{CAC}, or t_{AA} (whichever occurs later), access time = t_{OE}.

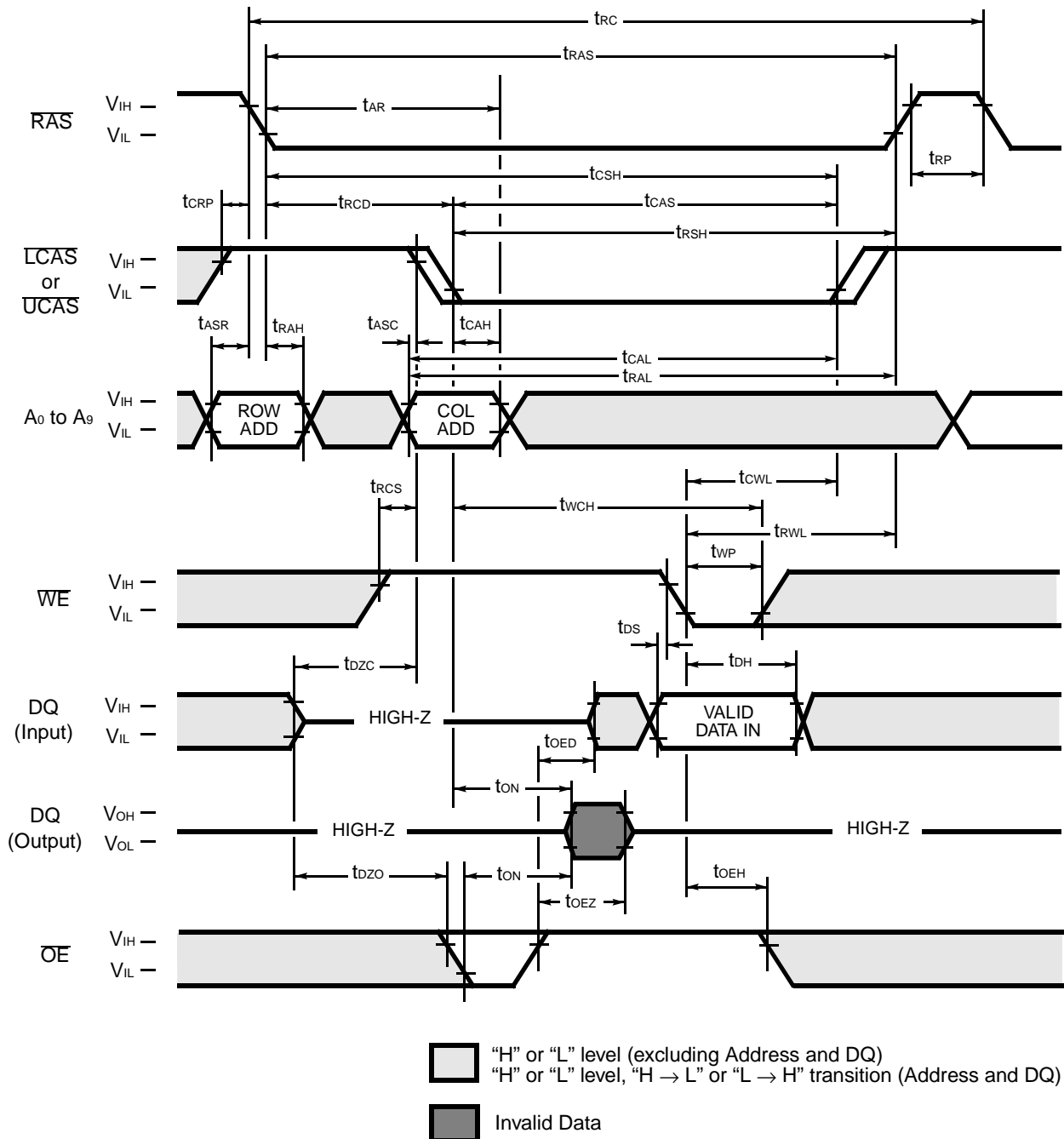
However, if either LCAS/UCAS or OE goes High, the output returns to a high-impedance state after t_{TOH} is satisfied.

MB8118160B-50/-60

Fig. 6 – EARLY WRITE CYCLE (\overline{OE} = “H” or “L”)**DESCRIPTION**

A write cycle is similar to a read cycle except \overline{WE} is set to a Low state and \overline{OE} is an “H” or “L” signal. A write cycle can be implemented in either of three ways—early write, delayed write, or read-modify-write. During all write cycles, timing parameters t_{RWL} , t_{CWL} , t_{RAL} and t_{CAL} must be satisfied. In the early write cycle shown above t_{WCS} is satisfied, data on the DQ pins are latched with the falling edge of \overline{LCAS} or \overline{UCAS} and written into memory.

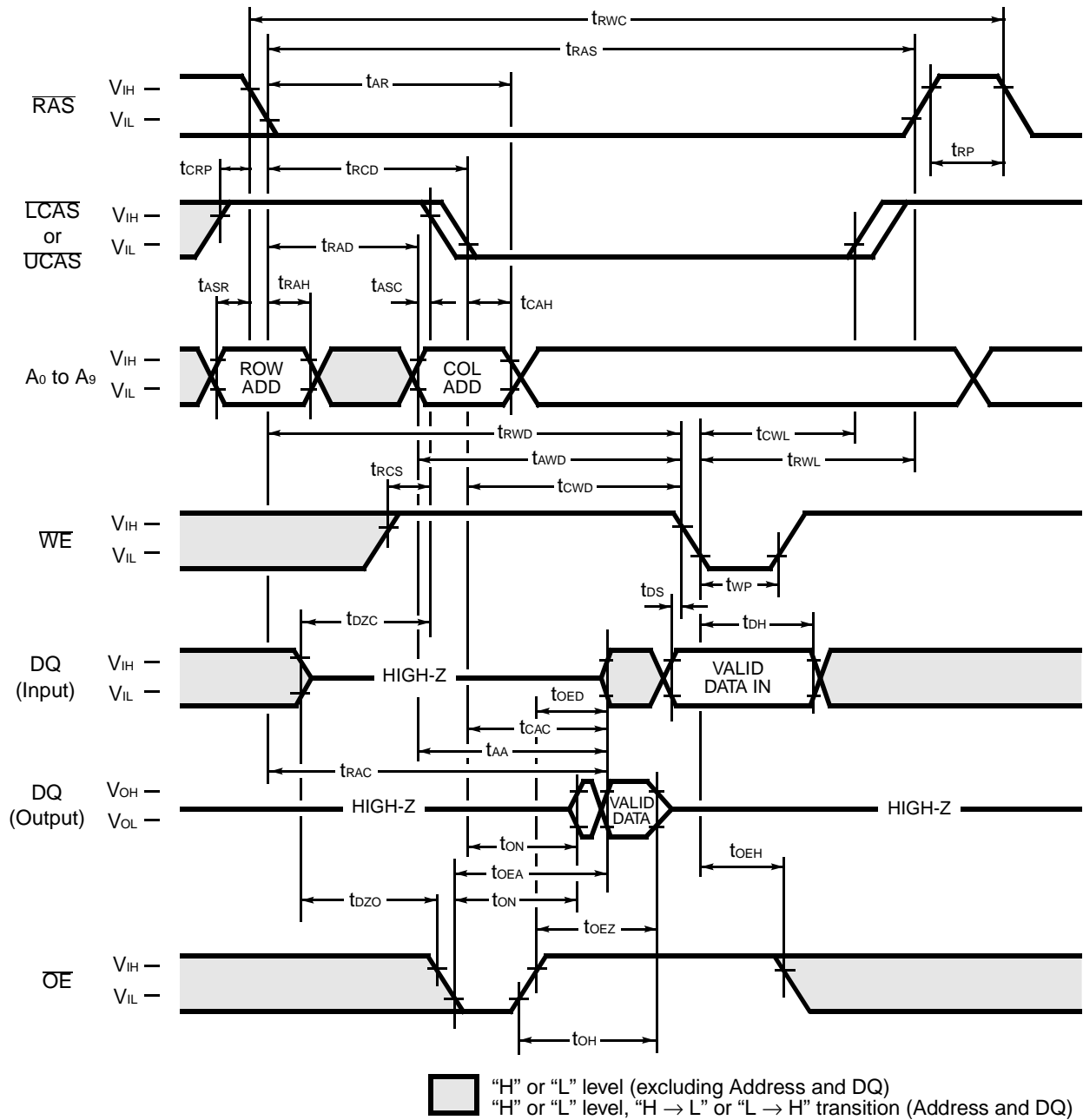
Fig. 7 - DELAYED WRITE CYCLE

**DESCRIPTION**

In the delayed write cycle, t_{WCS} is not satisfied; thus, the data on the DQ pins is latched with the falling edge of \overline{WE} and written into memory. The Output Enable (\overline{OE}) signal must be changed from Low to High before \overline{WE} goes Low ($t_{OED} + t_r + t_{DS}$).

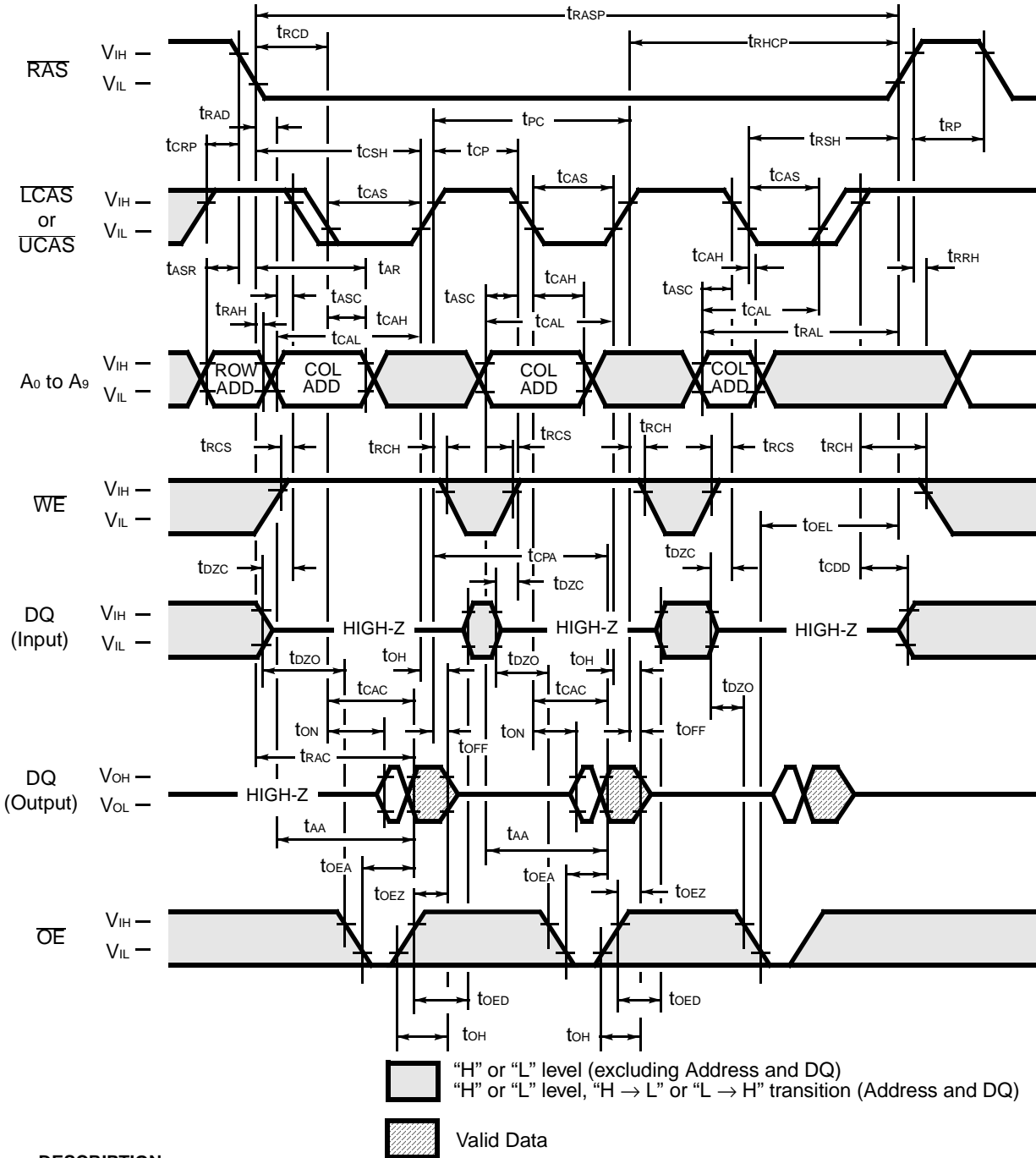
MB8118160B-50/-60

Fig. 8 – READ-MODIFY-WRITE CYCLE

**DESCRIPTION**

The read-modify-write cycle is executed by changing \overline{WE} from High to Low after the data appears on the DQ pins. In the read-modify-write cycle, \overline{OE} must be changed from Low to High after the memory access time.

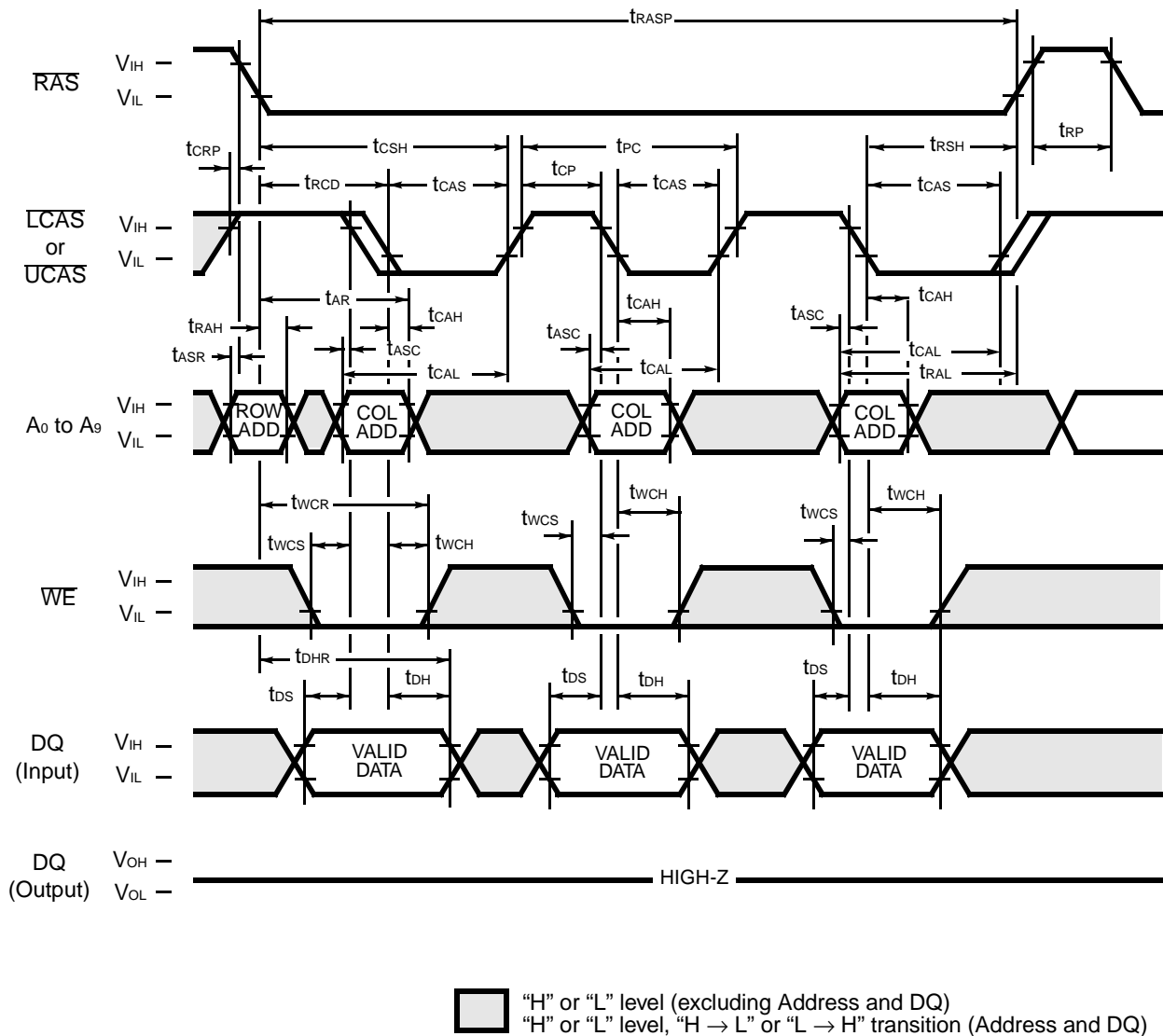
Fig. 9 – FAST PAGE MODE READ CYCLE



DESCRIPTION

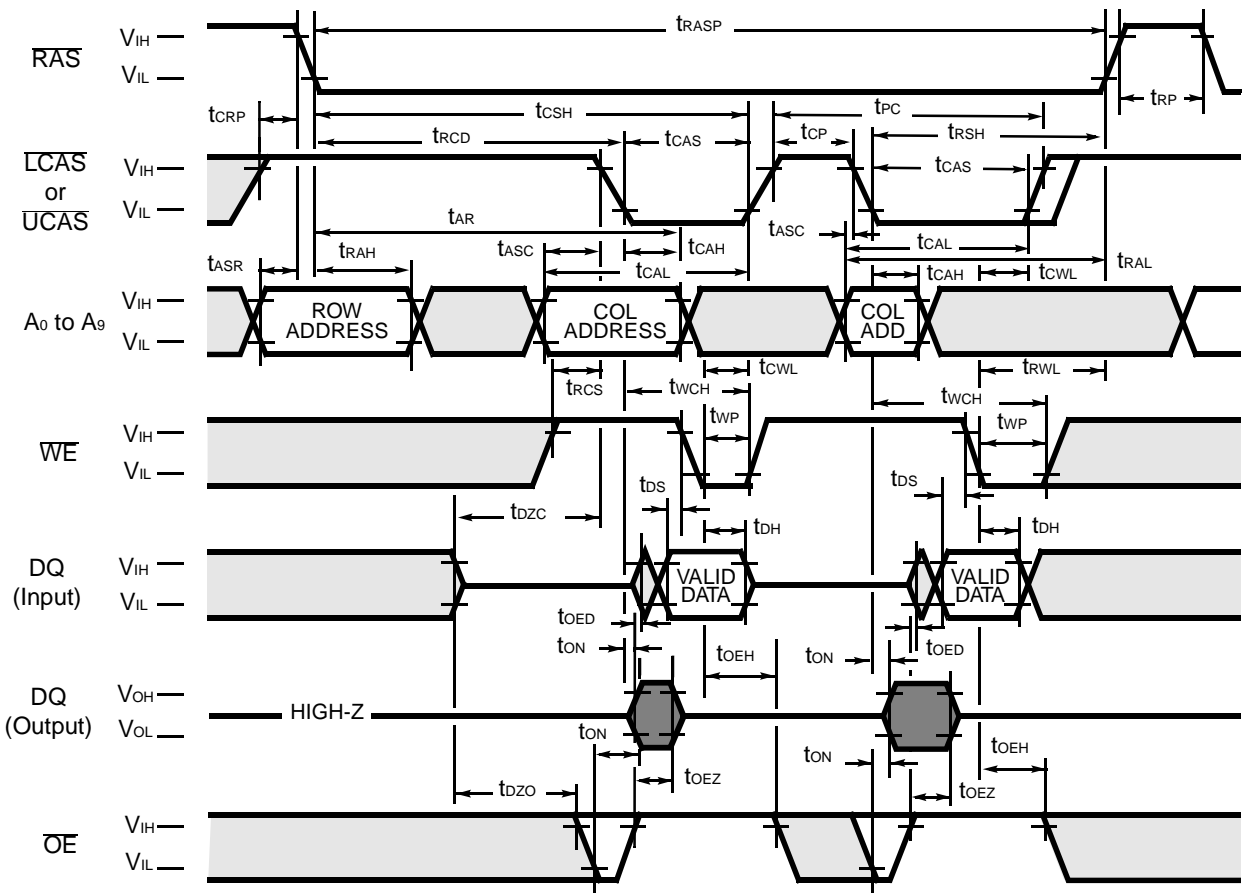
The fast page mode of operation permits faster successive memory operations at multiple column locations of the same row address. This operation is performed by strobing in the row address and maintaining RAS at a Low level and WE at a High level during all successive memory cycles in which the row address is latched. The address time is determined by t_{CAC} , t_{AA} , t_{CPA} , or t_{OEA} , whichever one is the latest in occurring.

MB8118160B-50/-60

Fig. 10 – FAST PAGE MODE EARLY WRITE CYCLE (\overline{OE} = “H” or “L”)**DESCRIPTION**

The fast page mode early write cycle is executed in the same manner as the fast page mode read cycle except the states of \overline{WE} and \overline{OE} are reversed. Data appearing on the DQ_1 to DQ_8 is latched on the falling edge of \overline{LCAS} and one appearing on the DQ_9 to DQ_{16} is latched on the falling edge of \overline{UCAS} and the data is written into the memory. During the fast page mode early write cycle, including the delayed (\overline{OE}) write and read-modify-write cycles, t_{wCL} must be satisfied.

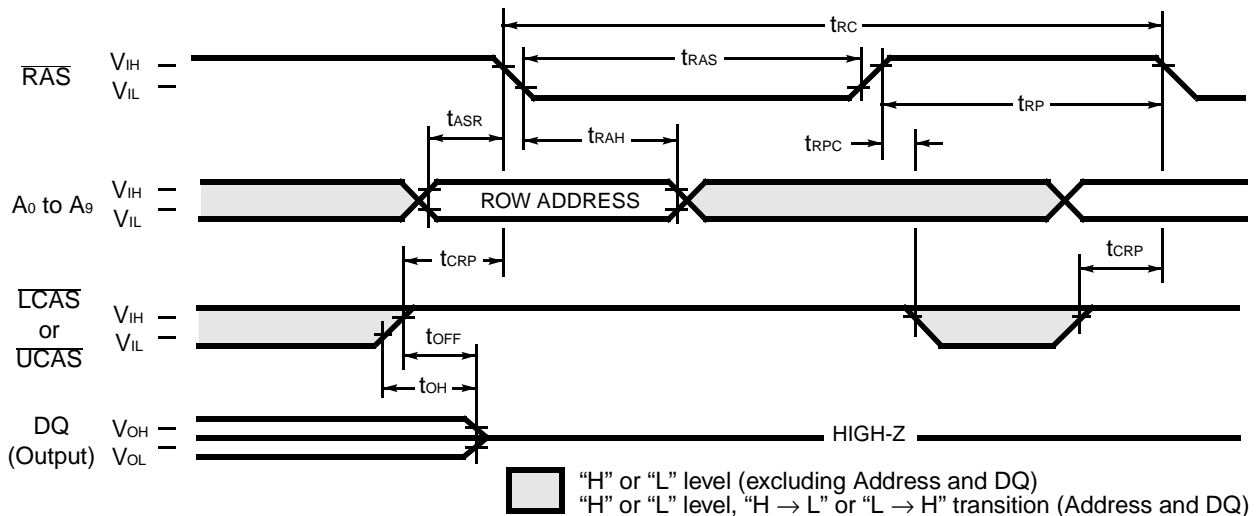
Fig. 11 – FAST PAGE MODE DELAYED WRITE CYCLE



- “H” or “L” level (excluding Address and DQ)
- “H” or “L” level, “H → L” or “L → H” transition (Address and DQ)
- Invalid Data

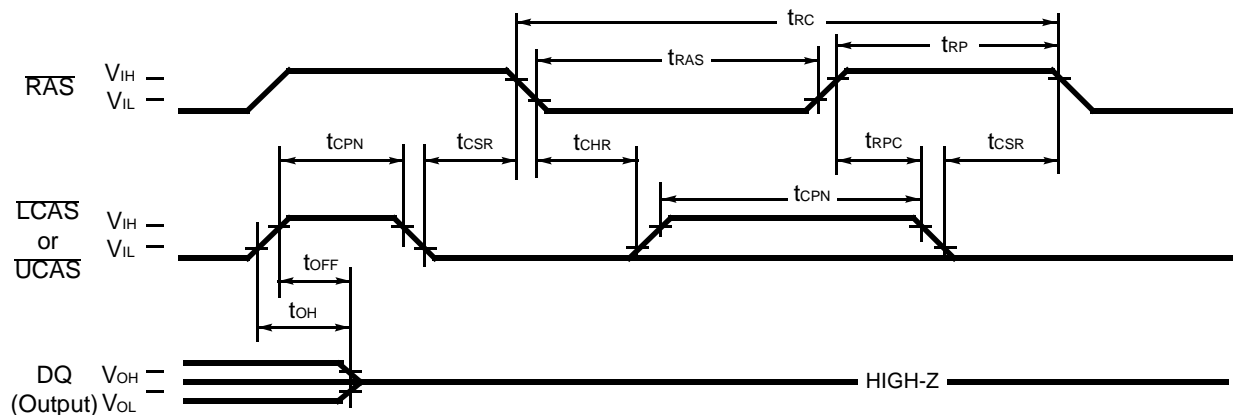
DESCRIPTION

The fast page mode delayed write cycle is executed in the same manner as the fast page mode early write cycle except for the states of WE and OE. Input data on the DQ pins are latched on the falling edge of WE and written into memory. In the fast page mode delayed write cycle, OE must be changed from Low to High before WE goes Low ($t_{OED} + t_r + t_{DS}$).

Fig. 13 - RAS-ONLY REFRESH ($\overline{WE} = \overline{OE} = \text{"H" or "L"}$)**DESCRIPTION**

Refresh of RAM memory cells is accomplished by performing a read, a write, or a read-modify-write cycle at each of 1,024 row addresses every 16.4-milliseconds. Three refresh modes are available: RAS-only refresh, CAS-before-RAS refresh, and hidden refresh.

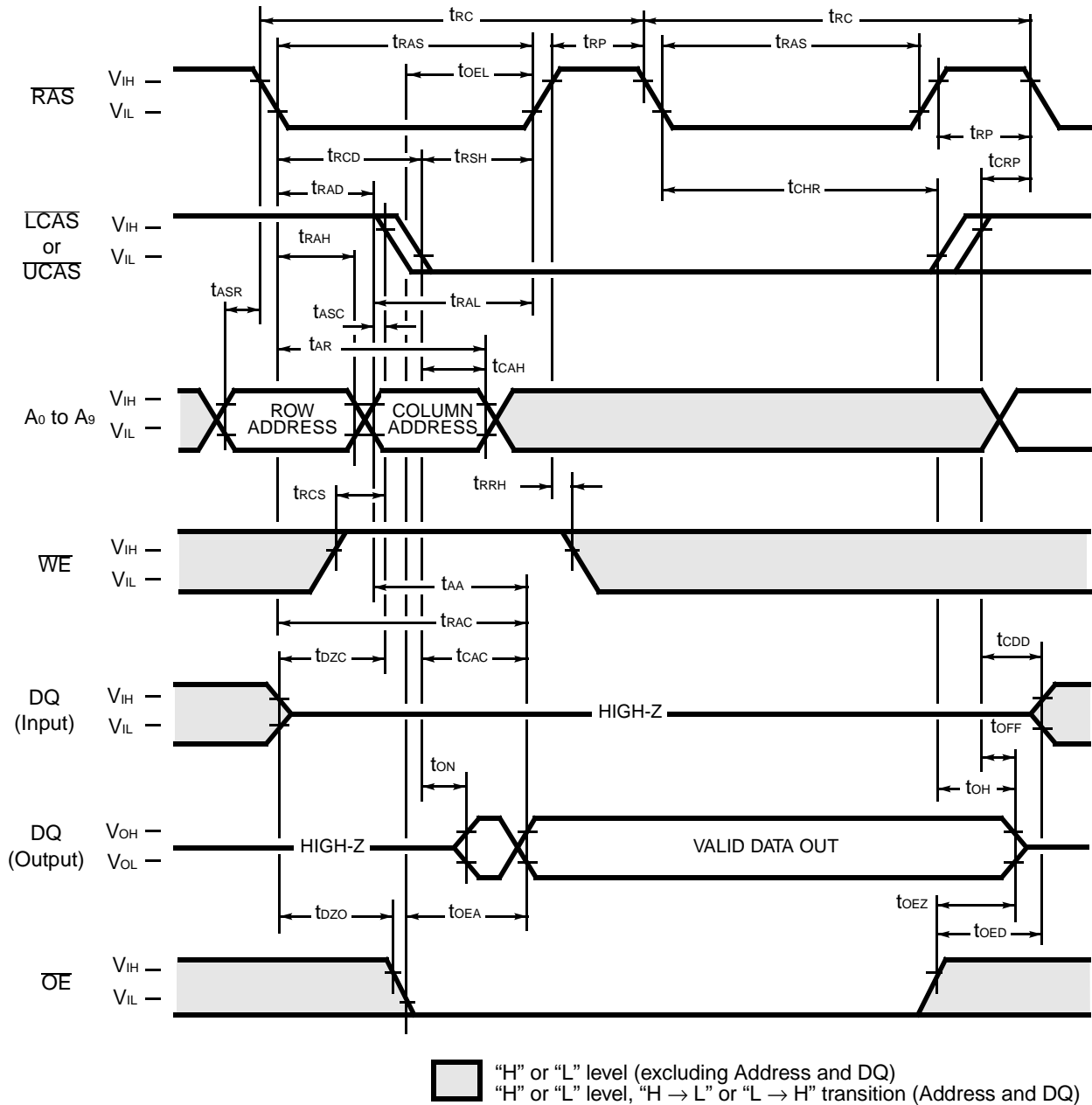
RAS-only refresh is performed by keeping RAS Low and LCAS and UCAS High throughout the cycle; the row address to be refreshed is latched on the falling edge of RAS. During RAS-only refresh, DQ pins are kept in a high-impedance state.

Fig. 14 - CAS-BEFORE-RAS REFRESH (ADDRESSES = $\overline{WE} = \overline{OE} = \text{"H" or "L"}$)**DESCRIPTION**

CAS-before-RAS refresh is an on-chip refresh capability that eliminates the need for external refresh addresses. If LCAS or UCAS is held Low for the specified setup time (t_{CSR}) before RAS goes Low, the on-chip refresh control clock generators and refresh address counter are enabled. An internal refresh operation automatically occurs and the refresh address counter is internally incremented in preparation for the next CAS-before-RAS refresh operation.

MB8118160B-50/-60

Fig. 15 – HIDDEN REFRESH CYCLE

**DESCRIPTION**

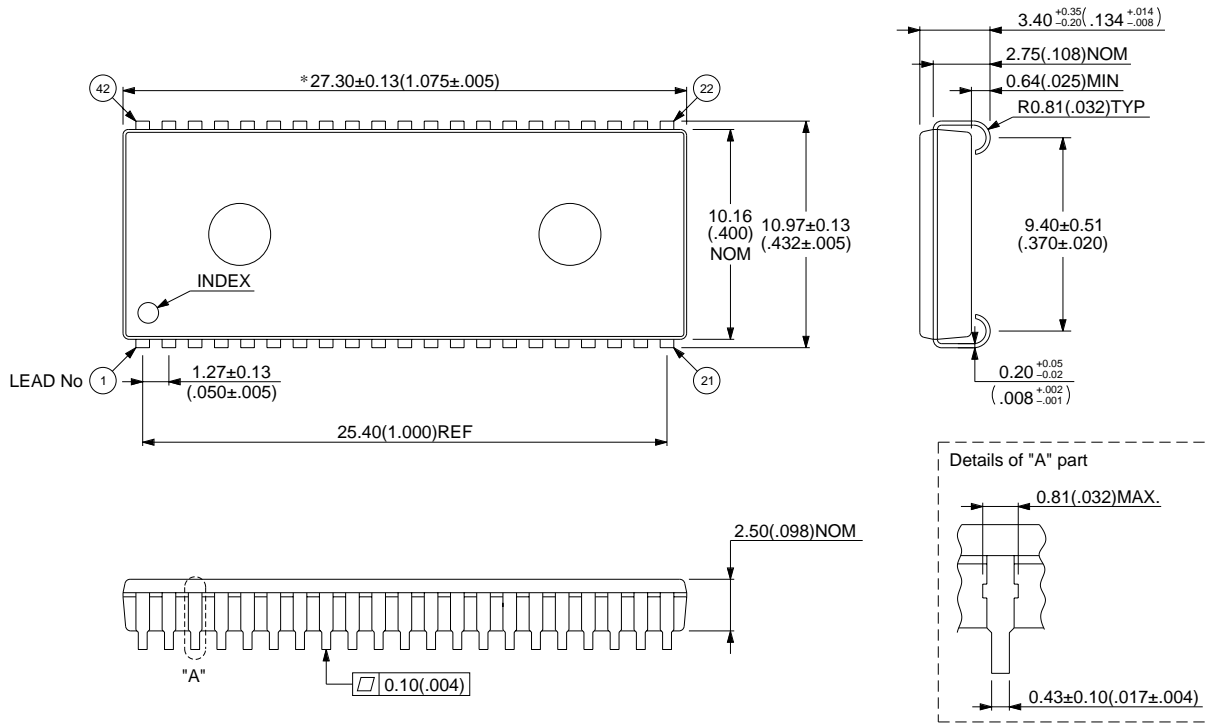
A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the active time of $\overline{\text{LCAS}}$ or $\overline{\text{UCAS}}$ and cycling RAS. The refresh row address is provided by the on-chip refresh address counter. This eliminates the need for the external row address that is required by DRAMs that do not have $\overline{\text{CAS}}$ -before-RAS refresh capability.

MB8118160B-50/-60

■ PACKAGE DIMENSIONS

42-pin plastic SOJ
(LCC-42P-M01)

*: Resin protrusion. (Each side:0.15(.006)MAX.)



© 1995 FUJITSU LIMITED C42001S-2C-1

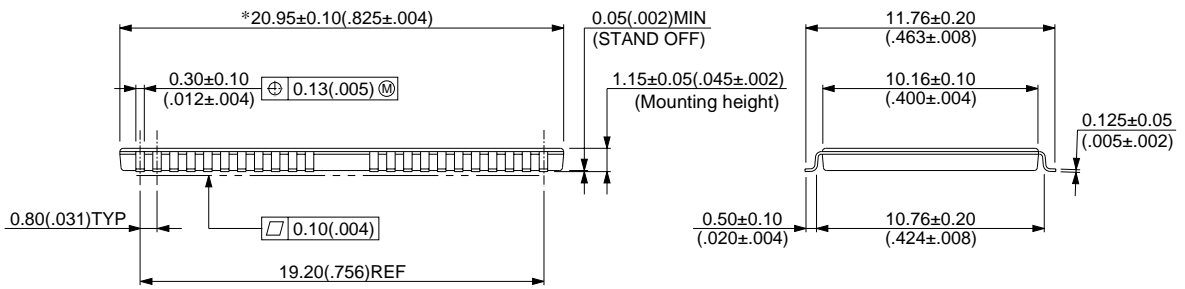
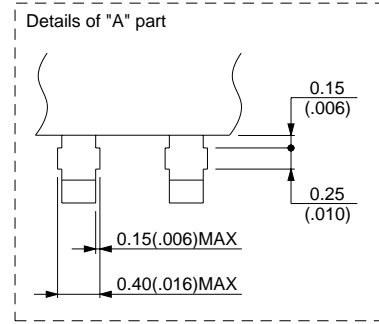
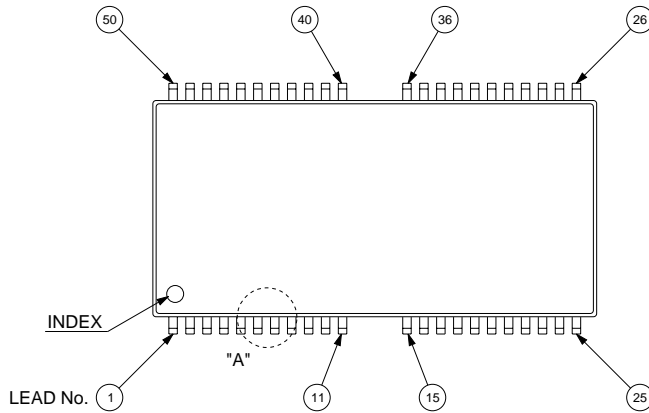
Dimensions in mm (inches)

MB8118160B-50/-60

(Continued)

50-pin plastic TSOP (II) (FPT-50P-M06)

*: Resin protrusion. (Each side:0.15(.006)MAX.)



© 1994 FUJITSU LIMITED F50006S-2C-1

Dimensions in mm (inches)

MB8118160B-50/-60

FUJITSU LIMITED

For further information please contact:

Japan

FUJITSU LIMITED
Corporate Global Business Support Division
Electronic Devices
KAWASAKI PLANT, 4-1-1, Kamikodanaka
Nakahara-ku, Kawasaki-shi
Kanagawa 211-88, Japan
Tel: (044) 754-3763
Fax: (044) 754-3329

<http://www.fujitsu.co.jp/>

North and South America

FUJITSU MICROELECTRONICS, INC.
Semiconductor Division
3545 North First Street
San Jose, CA 95134-1804, U.S.A.
Tel: (408) 922-9000
Fax: (408) 922-9179

Customer Response Center
Mon. - Fri.: 7 am - 5 pm (PST)
Tel: (800) 866-8608
Fax: (408) 922-9179

<http://www.fujitsumicro.com/>

Europe

FUJITSU MIKROELEKTRONIK GmbH
Am Siebenstein 6-10
D-63303 Dreieich-Buchsschlag
Germany
Tel: (06103) 690-0
Fax: (06103) 690-122

<http://www.fujitsu-edo.com/>

Asia Pacific

FUJITSU MICROELECTRONICS ASIA PTE LTD
#05-08, 151 Lorong Chuan
New Tech Park
Singapore 556741
Tel: (65) 281-0770
Fax: (65) 281-0220

<http://www.fmap.com.sg/>

F9712

© FUJITSU LIMITED Printed in Japan

All Rights Reserved.

The contents of this document are subject to change without notice. Customers are advised to consult with FUJITSU sales representatives before ordering.

The information and circuit diagrams in this document presented as examples of semiconductor device applications, and are not intended to be incorporated in devices for actual use. Also, FUJITSU is unable to assume responsibility for infringement of any patent rights or other rights of third parties arising from the use of this information or circuit diagrams.

FUJITSU semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION:

Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with FUJITSU sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Control Law of Japan, the prior authorization by Japanese government should be required for export of those products from Japan.